REMARKS

Claims 1-10, 15-34, and 38-42 remain pending in the current Application. Non-elected claims 11-14 and 35-37 have been cancelled without prejudice. Claims 1, 5, 15, 19, 20, 26, and 29 have been amended. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants have amended the specification in order to include a statement referring to the parent application.

Rejection of claims 1-3, 5, 8-10, 15, 19, and 23-25 under 35 U.S.C. 102(e)

Applicant respectfully submits that claims 1-3, 5, 8-10, 15, 19, and 23-25 are patentable over US Patent No. 6,245,641 (hereinafter referred to as Shiozawa).

Applicants have amended claims 1, 15, 26, and 29 to require that the first and second insulating layers are *grown*. Furthermore, claim 38, as originally presented, includes *growing* a first insulator liner in the first trench and a second insulator liner in the second trench. Also each of these claims (1, 15, 26, 29, 38) include etching a portion or at least a portion of the first insulator liner. Therefore, claims 1, 15, 26, 29, and 38 include etching a portion (or at least a portion) of the *grown* first insulator layer. The Examiner states that the first insulator liner is taught by layers 5b, 5c, and 8 of Shiozawa and that the second insulator liner is taught by 5a and 8 of Shiozawa. However, Applicants respectfully disagree. Although portions 5a, 5b, and 5c of Shiozawa are thermal oxides, silicon oxide film 8, as stated in col. 10, lines 5-10, of Shiozawa is deposited by CVD and not grown. Furthermore, silicon oxide film 8 of Shiozawa cannot be grown since it must also be formed on the silicon nitride films 3a to 3d in order to prevent corner erosion of the nitride films 3a and 3b during the trench fill process (see col. 10, lines 5-10 and lines 45-65, of Shiozawa). Unlike claims 1, 15, 26, 29, and 38, only the silicon oxide film 8 of

the oxide layers of Shiozawa is ever removed (see FIG.7). That is, Shiozawa does not teach or even suggest the etching of a *grown* oxide within the trenches. Therefore, for at least those reasons, Applicants submit that claims 1, 15, 26, 29, and 38 are patentable over Shiozawa. Claims 2-10, 16-25, 27-28, 30-34, and 39-42 have not been independently addressed because they depend directly or indirectly from allowable claims 1, 15, 26, 29, or 38, and are therefore allowable for at least those reasons stated above with respect to these claims.

Conclusion

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 502117.

Respectfully submitted,

By: _____

Joanna G. Chiu
Attorney of Record
Reg. No.: 43,629
Telephone: (512) 996-6839
Fax No.: (512) 996-6854

SEND CORRESPONDENCE TO:

Motorola, Inc.
Law Department

Customer Number: 23125

CLAIMS - VERSION WITH MARKINGS TO SHOW CHANGES MADE

(note -- a full set of claims is being provided for the convenience of the Examiner, *but only claims 1, 5, 15, 19, 20, 26, and 29 have been amended herein.*)

1. **(Amended)** A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width and a second trench of a second width in the semiconductor layer;

[forming] growing a first insulator liner in the first trench and a second insulator liner in the second trench;

forming a mask over the second trench;

etching at least a portion of the first insulator liner while the mask is over the second trench;

removing the mask; and

depositing an insulating layer in the first trench and the second trench.

2. The method of claim 1, wherein the first width is less than the second width.

3. The method of claim 1, wherein the step of etching comprises completely removing the first insulator liner.

4. The method of claim 1, wherein the step of etching results in leaving at least one hundred Angstroms of the first insulator liner.

5. **(Amended)** The method of claim 1, wherein the step of [forming] growing the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

6. The method of claim 1, wherein the step of etching comprises dipping the semiconductor device structure in hydrofluoric acid.

7. The method of claim 1, wherein the step of etching comprises applying a dry etch chemistry to the semiconductor device structure.

8. The method of claim 1, wherein the insulator layer comprises high density plasma oxide fill.

9. The method of claim 1, further comprising forming a barrier layer and a stress relief layer over the semiconductor layer in areas adjacent to the first trench and the second trench.

10. The method of claim 1, further comprising forming a pad nitride and pad oxide over the semiconductor layer prior to forming the first trench and the second trench, and wherein the step of forming the first trench and the second trench comprises etching through selected portions of the pad nitride and the pad oxide and into the semiconductor layer.

15. (**Amended**) A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width and a second trench of a second width in the semiconductor layer, the first width being less than the second width;

[forming] growing a first insulator liner in the first trench and a second insulator liner in the second trench;

forming a mask over the second trench; and

etching at least a portion of the first insulator liner while the mask is over the second trench.

16. The method of claim 15, wherein the step of etching comprises a wet etch.

17. The method of claim 16, wherein the step of etching comprises dipping the semiconductor device structure in hydrofluoric acid.

18. The method of claim 15, wherein the etching comprises a dry etch.

19. (**Amended**) The method of claim 15, wherein the step of [forming] growing the first insulator liner and the second insulator liner comprises growing oxide in the first trench and the second trench.

20. (**Amended**) The method of claim 15, wherein:

the semiconductor layer has a top surface;

the second trench has a corner where the trench adjoins the top surface of the semiconductor layer; and

the step of [forming] growing the first insulator liner and the second insulator liner comprises rounding of the corner of the second trench.

21. The method of claim 20, wherein the corner is semiconductor.

22. The method of claim 15, wherein the step of etching comprises leaving at least 100 Angstroms of the first insulating liner.

23. The method of claim 15, wherein the step of etching comprises removing the first insulating liner.

24. The method of claim 15, further comprising forming a barrier layer and a stress relief layer over the semiconductor layer in areas adjacent to the first trench and the second trench.

25. The method of claim 24, wherein the barrier layer comprises nitride and the stress relief layer comprises oxide.

26. (**Amended**) A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width in the semiconductor layer;

forming a second trench of a second width greater than the first width in the second semiconductor layer;

[forming] growing a first insulator liner in the first trench and a second insulator liner in the second trench;

etching a portion of the first insulator liner; and

depositing an insulating layer in the first trench.

27. The method of claim 26 further comprising

forming a mask over the second trench prior to the step of etching; and

removing the mask prior to the step of depositing.

28. The method of claim 26, wherein the step of etching further comprises etching a portion of the second insulator liner and leaves at least 50 Angstroms of the first insulator liner and 50 Angstroms of the second liner.

29. (**Amended**) A method for forming a semiconductor device structure in a semiconductor layer, comprising:

forming a first trench of a first width in the semiconductor layer;

forming a second trench of a second width in the second semiconductor layer;

[forming] growing a first insulator liner in the first trench and a second insulator liner in the second trench;

etching a portion of the first insulator liner and a portion of the second insulator liner; and

depositing an insulating layer in the first trench and the second trench.

30. The method of claim 29, wherein the step of etching comprises a wet etch.

31. The method of claim 30, wherein the wet etch uses hydrofluoric acid.

32. The method of claim 29, wherein the first insulator and the second insulator liner comprises thermal oxide.

33. The method of claim 29, wherein the step of depositing comprises filling the first trench and second trench.

34. The method of claim 33, wherein the insulating layer comprises high density plasma oxide.

38. A method for forming a semiconductor device structure in a semiconductor layer having a top surface, comprising:

forming a first trench of a first width in the semiconductor layer and having a first corner at the surface of the semiconductor layer;

forming a second trench of a second width greater than the first trench in the second semiconductor layer and having a second corner at the surface of the semiconductor layer;

growing a first insulator liner in the first trench and a second insulator liner in the second trench to achieve a radius of curvature of at least 200 Angstroms in the first and second corner;

etching a portion of the first insulator liner and a portion of the second insulator liner; and

depositing an insulating layer in the first trench and the second trench that fills the first and second trenches, wherein the insulating layer is free of voids.

39. The method of claim 38, wherein the first insulator liner and the second insulator liner are thermal oxide.

40. The method of claim 38, wherein the step of etching leaves the first insulator liner and the second insulator liner at a thickness sufficiently small to allow for completely filling the first trench with the insulating layer without voids in the insulating layer.

41. The method of claim 40, wherein the insulating layer comprises high density plasma oxide.

42. The method of claim 38, wherein the step of etching is further characterized as leaving at least 50 Angstroms of the first insulator liner and the second insulator liner.